AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An interconnect structure comprising

a contact dielectric layer comprising a first undoped silicon oxide;

an etch stop layer comprising a doped silicon oxide over the contact dielectric layer;

a trench dielectric layer comprising a second undoped silicon oxide over the etch stop layer; and

an electrically conductive interconnect in (i) a hole through the contact dielectric layer and the etch stop layer, and (ii) a trench in the trench dielectric layer~~, wherein~~

~~the etch stop layer comprises one member selected from a group consisting of an undoped silicon oxide and a doped silicon oxide, and each of the contact dielectric layer and the trench dielectric layer independently comprises the other member of the group~~.

Claims 2-4 (Canceled).

5. (Original) The interconnect structure according to Claim 1, wherein the trench in the trench dielectric layer is wider than the hole through the etch stop and contact dielectric layers.

6. (Original) The interconnect structure according to Claim 1, further comprising

a substrate; and

a gate structure on the substrate in contact with the contact dielectric layer.

7. (Original) The interconnect structure according to Claim 6, wherein the substrate comprises silicon.

8. (Original) The interconnect structure according to Claim 6, wherein the gate structure comprises a gate dielectric layer over the substrate, a gate over the gate dielectric layer, a cap dielectric layer over the gate, and spacers adjacent to the gate and the cap dielectric layer.

9. (Original) The interconnect structure according to Claim 1, wherein the electrically conductive interconnect comprises a member selected from the group consisting of Al and Cu.

10. (Original) The interconnect structure according to Claim 1, wherein a thickness of the etch stop layer is from 100 Å to 1000 Å.

Claims 11-18 (Canceled).

19. (Currently Amended) A method of forming an interconnect structure, the method comprising

providing a contact dielectric layer, an etch stop layer over the contact dielectric layer, and a trench dielectric layer over the etch stop layer;

etching a hole through the contact dielectric layer and the etch stop layer;

etching a trench in the ~~trenching~~ trench dielectric layer;

introducing an electrically conductive interconnect into the hole and the trench; and

producing the interconnect structure of Claim 1.

SUPPORT FOR THE AMENDMENT

This Amendment cancels Claims 2-4 and 18; and amends Claims 1 and 19. Support for the amendments is found in the specification and claims as originally filed. In particular, support for Claim 1 is found in canceled Claim 18. No new matter would be introduced by entry of these amendments.

Upon entry of these amendments, Claims 1, 5-10 and 19 will be pending in this application. Claim 1 is independent. Claim 19 is withdrawn from consideration.

REQUEST FOR RECONSIDERATION

Applicants respectfully request entry of the foregoing and reexamination and reconsideration of the application, as amended, in light of the remarks that follow.

Applicants thank the Examiner for the courtesies extended to their representative during the June 19, 2003, personal interview.

As discussed at the interview, the present invention provides an interconnect structure for wiring integrated circuits using a trench dielectric layer, an etch stop layer and a contact dielectric layer all containing undoped or doped silicon oxide. $C_2H_2F_4$ etch chemistry is used to selectively etch the undoped and doped silicon oxide layers. The exclusive use of silicon oxide in the trench dielectric, etch stop and contact dielectric layers results in a significant reduction in total dielectric constant relative to conventional interconnect structures including a layer of silicon nitride.

Claims 1-5 and 9-10 are rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,313,025 ("Chittipeddi"). In addition, Claims 6-8 are rejected under 35 U.S.C. § 103(a) over Chittipeddi in view of U.S. Patent No. 6,130,102 ("White").

Chittipeddi discloses a dual damacene structure including a first insulating layer 105, an etch stop layer 110 formed above or in direct contact with the first insulating layer 105, and a second insulating layer 115 above or in direct contact with the etch stop layer 110. The etch stop layer may be a silicon-rich oxide or a multi-layered SiO_2 dielectric. See, Chittipeddi at column 3, lines 18-21.

White is cited for disclosing the gate structures of Claims 6-8.

At least because Chittipeddi is silent about doping an etch stop layer of silicon oxide, Claim 18, which features an etch stop layer comprising doped silicon oxide, is not rejected over prior art. Claim 18 is canceled and incorporated into independent Claim 1. Because the cited prior art fails to suggest the independent Claim 1 limitation of "an etch stop layer comprising a doped silicon oxide", the rejections under 35 U.S.C. §§ 102(e) and 103(a) should be withdrawn.

Claims 1-10 and 18 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Office Action asserts that the independent Claim 1 feature of an etch stop layer comprising a doped silicon oxide "is not enabled because the specification described that the etch stop layer is an undoped silicon oxide". Office Action at page 3, section 6.

However, the specification also discloses that the etch stop layer can be doped silicon oxide. For example, the specification discloses:

> The present invention provides a dual damacene structure in which a conventional etched top layer (e.g., of silicon nitride) is replaced with an **etch stop layer** of either **doped** or undoped **silicon oxide**. If the etch stop layer is a **doped silicon oxide**, then the dielectric layers above and below the etch stop layer are undoped silicon oxide. If the etched stop layer is undoped silicon

> oxide, then the dielectric layers above and below the etch stop layer are doped silicon oxide. An etch chemistry containing $C_2H_2F_4$ (and optionally CHF_3) provides sufficient etch selectivity between undoped silicon oxide and various doped oxides for the undoped silicon oxide to act as an etch stop layer (***or vice versa***). Specification at page 4, lines 8-15 (emphasis added).

Furthermore, the specification at page 6, lines 12 ff., discloses $C_2H_2F_4$ etch chemistry in great detail.

As discussed in MPEP § 2164.04:

> In order to make a rejection, the Examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. ... A specification disclosure which contains a teaching of the manner and process of making and using an invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as being in compliance with the enablement requirement of 35 U.S.C. §112, first paragraph, unless there is a reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support. ... As stated by the court "it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain *why* it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement. Otherwise, there would be no need for the Applicant to go to the trouble and expense of supporting his presumptively accurately disclosure." MPEP § 2164.04, (italics in original).

Because the specification enables the skilled artisan to practice the claimed invention without undue experimentation, and the Patent Office has not met its burden of establishing a reasonable basis to question the enablement provided for the claimed invention, the rejection under 35 U.S.C. § 112, first paragraph, should be withdrawn.

Claims 1-10 are rejected under 35 U.S.C. § 112, second paragraph, because assertedly in Claim 1, line 1, the phrase "the other member of the group" renders the claim indefinite. To obviate the rejection, Claim 1 is amended.

Pursuant to MPEP § 821.04, after independent product Claim 1 is allowed, Applicants respectfully request rejoinder, examination and allowance of withdrawn method Claim 19, which includes all the limitations of independent product Claim 1.

The Office Action objects to the title of the invention as not being descriptive and asserts that a new title is required that is clearly indicative of the invention to which the claims are directed. However, in view of and following the rejoinder of method Claim 19 to the pending product claims, Applicants respectfully submit that the title of the invention "Dual Damascene Structure and Method of Making" is clearly indicative of the invention to which the claims are directed. Thus, the objection to the title should be withdrawn.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance. Applicants respectfully request favorable consideration and prompt allowance of the application.

Should the Examiner believe that anything further is necessary in order place the application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Corwin Paul Umbach

Richard L. Chinn, Ph.D.
Registration No. 34,305
Attorney of Record

Corwin P. Umbach, Ph.D.
Registration No. 40,211

Customer Number
22850
(703) 413-3000
Fax #: (703) 413-2220

NFO/CPU:smi